Amendments to the Specification:

Please replace the paragraph beginning on page 3 at line 6 with the following amended paragraph:

According to one aspect of the present invention, there is provided a method of providing synchronized clock signals at "n N" distributed nodes in a synchronous system, the nodes comprising a master node and a plurality of slave nodes interconnected by first and second propagation channels. The method comprises the steps of:

at the master node,

(i) generating a first pulse train and a second pulse train each being regular and having a period (T),

(ii) propagating the first pulse train around the plurality of slave nodes via the first propagation channel;

(iii) propagating the second train of pulses around the plurality of slave nodes via the second propagation channel such that the pulses of the second train of pulses arrive at respective ones of the plurality of slave nodes in reverse order to the pulses of the first pulse train; and

~~(iii)~~(iv) maintaining the rate of each of the first and second pulse trains such that there are "~~pn~~ pN" pulses in each propagation channel at any time, where "n N" is the number of nodes, including the master node, and "p" is an integer, the pulses of the first train of pulses arrive at respective ones of the plurality of slave nodes substantially simultaneously, and the pulses of the second train of pulses arrive at respective ones of the plurality of slave nodes substantially simultaneously; and

at each of the slave nodes,

~~(iv)~~(v) detecting arrival at a predetermined detection point of a pair of pulses, the pair comprising one pulse from each of the first pulse train and the second pulse train; and

~~(v)~~(vi) generating a clock signal event in dependence upon the pair of pulses both arriving at the detection point with a phase difference below a preset level.

Please replace the paragraph beginning on page 4 at line 24 with the following amended paragraph:

According to a second aspect of the invention, there is provided apparatus for providing synchronized clock signals at "n N" distributed nodes in a synchronous system, the apparatus comprising a master node unit and a plurality of slave node units interconnected in series by first and second propagation ~~paths~~ channels, the master node unit comprising:

pulse generation means for providing a first pulse train and a second pulse train, the pulse trains each being regular and both having the same period;
means for propagating the first pulse train around the slave nodes via the first propagation channel and the second pulse train around the slave nodes via the second propagation channel; and
means for maintaining the rate of the first pulse train and second pulse train such that, at any instant, there are "~~pn~~ pN" pulses in each propagation channel, where "~~n~~ N" is the number of nodes, including the master node, and "p" is an integer; and such that the pulses of the second pulse train arrive at respective ones of the plurality of slave nodes substantially simultaneously and the pulses of the first pulse train arrive at respective ones of the plurality of slave nodes substantially simultaneously, but in reverse order to the first pulse train ;
each of the slave node units comprising:
detection means for detecting arrival at a predetermined detection point of a pair of pulses comprising one pulse from each of the first pulse train and the second pulse train, respectively, and generating a clock signal event in dependence upon the phase difference between the pair of pulses being less than a preset level.

Please replace the paragraph beginning on page 12 at line 3 with the following amended paragraph:

Referring to Figure 3, slave node ~~N2~~ N2 has three pairs of electrical variable delay units, one pair in each of the three pulse propagation paths A, B and C. Each pair comprises a PRE-delay and a POST-delay. The "fast" paths A and B have "PRE" delays PRE2A and PRE2B, respectively, which are upstream of the detection points D2A and D2B, respectively, in the propagation direction, and "POST" delays POST2A and POST2B, respectively, which are downstream of the detection points D2A and D2B, respectively. The "slow" path C has delays PRE2C and POST2C which are similar to those in paths A and B, but they have no detection point between them, since the slow pulses are not detected in the slave nodes. It should be appreciated that changes to the delays in the "fast" paths A and B will affect their overall effective length or transmission time. Providing similar delays in the "slow" path C, and adjusting them along with those in the "fast" paths A and B, ensures that the overall effective length or transmission time of the "slow" path changes too, and causes the master node N1 to make a corresponding change in the pulse repetition rate, *vis*. by means of VCO 18.